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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/893,962	06/29/2001	Gee-Sung Chae	8733.487.00	6093

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EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/893,962	CHAE, GEE-SUNG	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *7-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-6 in the reply filed on 10/29/03 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U. S. Pat. 6,128,051) in view of Park et al. (U. S. Pat. 6.287.899 B1).

Kim et al. discloses an array substrate comprising a substrate; a first gate shorting bar 161 on the substrate, the first gate shorting bar 161 having a plurality of connectors 167; a second gate shorting bar 163 spaced apart from and parallel to the first gate shorting bar 161, the second gate shorting bar 163 having a plurality second connecting contact holes 169; a plurality of gate lines 113 on the substrate and perpendicular to the first and second gate shorting bars, the gate lines comprising odd numbered gate lines and even numbered gate lines , a plurality of gate pads 115 comprising odd numbered gate pads connected to the ends of odd numbered gate lines and even numbered gate pads connected to the ends of even numbered gate lines,

wherein each gate pad of said plurality of gate pads has a corresponding gate pad contact hole 151; a plurality of first pad connectors 167, each connecting an odd numbered gate pad to the first gate shorting bar via the corresponding gate pad contact hole and via a corresponding first connector; and a plurality of second pad connectors, each connecting an even numbered gate pad to the second gate shorting bar through the corresponding gate pad contact hole and via a corresponding second connecting contact hole.

Kim et al. discloses the claimed invention with the exception of the first gate shorting bar having a plurality of first connecting contact holes that connect the first gate shorting bar to the first pad connectors.

Park et al. discloses in fig. 2 an array substrate that comprises an array substrate comprising a substrate ; a first gate shorting bar 4 on the substrate, the first gate shorting bar having a plurality of first connecting contact holes 7; a second gate shorting bar 5 spaced apart from the first gate shorting bar, the second gate shorting bar having a plurality of second connecting contact holes 7, a plurality of gate lines 22 on the substrate and perpendicular to the first gate shorting bar; a plurality of gate pads 24 connected to the ends of the gate lines 22; and a plurality of first pad connectors 6, each connecting a gate pad to the first gate shorting bar via the corresponding gate pad contact hole and via a corresponding first connecting contact hole, wherein contact holes are used in the gate shorting bars for the disclosed intended purpose of making a discrete device that protects the device elements from electrostatic discharge failure.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use contact holes in the gate shorting bars to connect to the pad connectors for the disclosed intended purpose of obtaining discrete devices that more densely formed in the array while protecting the device elements from electrostatic discharge failure.

Kim et al. further discloses a plurality of data lines 123 that cross the plurality of gate lines so as to define a plurality of pixel regions; a plurality of thin film transistors, each film transistor having an associated pixel region; and a plurality of pixel electrodes, wherein each pixel electrode is located within an associated pixel region; wherein each thin film transistor includes a gate electrode, a source electrode, and a drain electrode; wherein the first pad connectors, the second pad connectors, and the plurality of pixel electrodes are formed of indium tin oxide.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. in view of Park et al. as applied to claims 1, 3-6 above, and further in view of Applicant's admitted prior art.

Kim et al. discloses an array substrate comprising a substrate; a first gate shorting bar 161 on the substrate, the first gate shorting bar 161 having a plurality of connectors 167; a second gate shorting bar 163 spaced apart from and parallel to the first gate shorting bar 161, the second gate shorting bar 163 having a plurality second connecting contact holes 169; a plurality of gate lines 113 on the substrate and perpendicular to the first and second gate shorting bars, the gate lines comprising odd

numbered gate lines and even numbered gate lines , a plurality of gate pads 115 comprising odd numbered gate pads connected to the ends of odd numbered gate lines and even numbered gate pads connected to the ends of even numbered gate lines, wherein each gate pad of said plurality of gate pads has a corresponding gate pad contact hole 151; a plurality of first pad connectors 167, each connecting an odd numbered gate pad to the first gate shorting bar via the corresponding gate pad contact hole and via a corresponding first connector; and a plurality of second pad connectors, each connecting an even numbered gate pad to the second gate shorting bar through the corresponding gate pad contact hole and via a corresponding second connecting contact hole.

Kim et al. discloses the claimed invention with the exception of the first gate shorting bar having a plurality of first connecting contact holes that connect the first gate shorting bar to the first pad connectors.

Park et al. discloses in fig. 2 an array substrate that comprises an array substrate comprising a substrate ; a first gate shorting bar 4 on the substrate, the first gate shorting bar having a plurality of first connecting contact holes 7; a second gate shorting bar 5 spaced apart from the first gate shorting bar, the second gate shorting bar having a plurality of second connecting contact holes 7, a plurality of gate lines 22 on the substrate and perpendicular to the first gate shorting bar; a plurality of gate pads 24 connected to the ends of the gate lines 22; and a plurality of first pad connectors 6, each connecting a gate pad to the first gate shorting bar via the corresponding gate pad

contact hole and via a corresponding first connecting contact hole, wherein contact holes are used in the gate shorting bars for the disclosed intended purpose of making a discrete device that protects the device elements from electrostatic discharge failure.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use contact holes in the gate shorting bars to connect to the pad connectors for the disclosed intended purpose of obtaining discrete devices that more densely formed in the array while protecting the device elements from electrostatic discharge failure.

Kim et al. as modified by Park et al. discloses the claimed invention including using aluminum for the gate lines and with the exception of using copper for the gate lines.

Applicant's admitted prior art discloses a substrate array that includes the use of copper for the gate lines instead of aluminum, for the well known purpose of eliminating electromigration and hillock problems that are associated with aluminum.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate lines of copper, as one of ordinary skill in the art would have used copper instead of aluminum for the well known purpose of eliminating electromigration and hillock problems that are associated with aluminum.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571)272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

PHAT X. CAO
PRIMARY EXAMINER